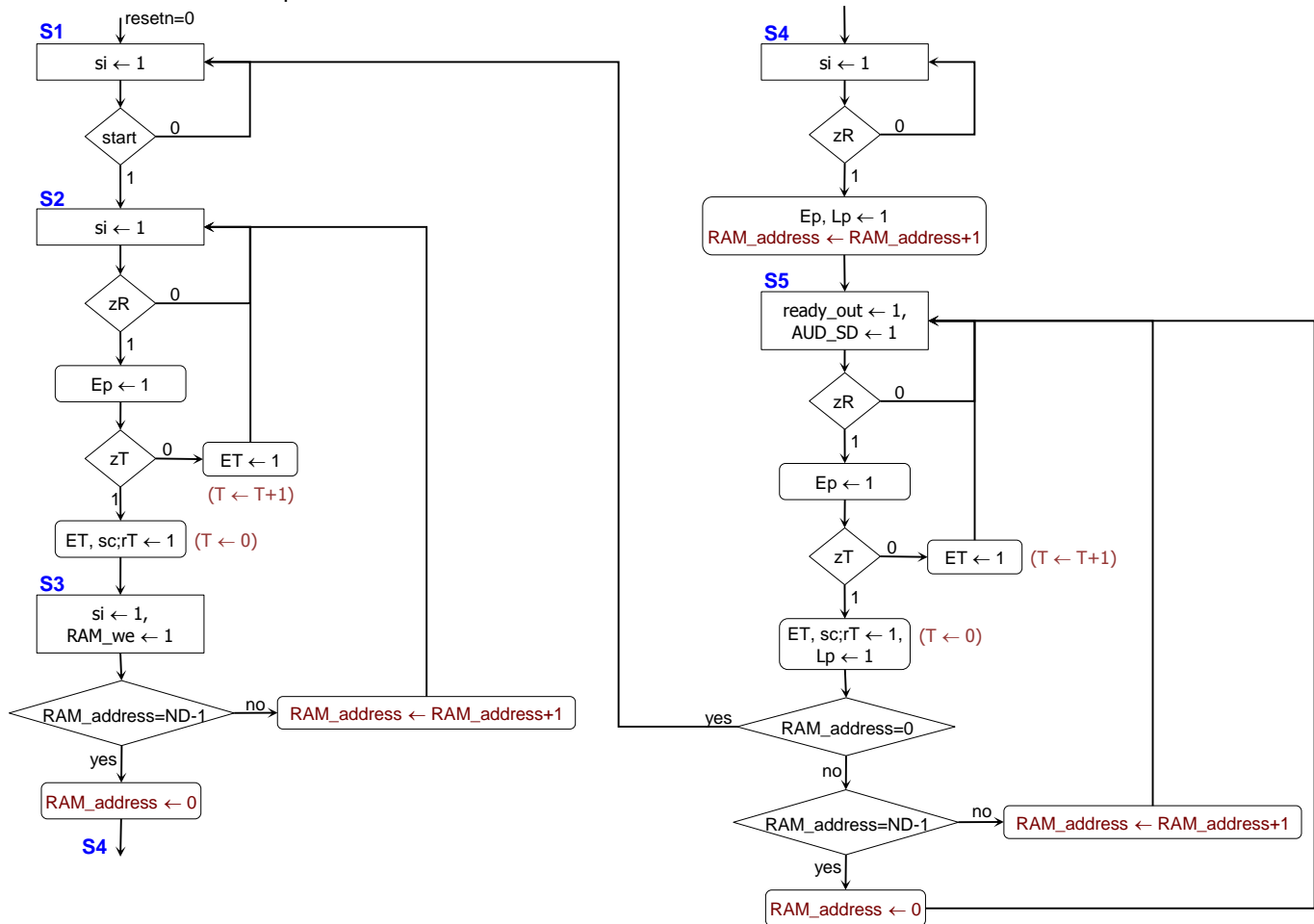


- **FSM_MEM:** This is the main controller. $ND = 512 \times 512 = 2^{18}$. This FSM embeds the counter `RAM_address`.
✓ Duration of the sequence: $2^{18} \times 16 \times 84 \times 10ns = 3.52 \text{ seconds}$.



- **VIVADO DESIGN FLOW FOR FPGAs – NEXYS A7-100T** (*A7-50T: use `nrows=512*256` as there is less memory)
✓ Create a new Vivado Project. Select the **XCA100T-1CSG324 Artix-7 FPGA**.
✓ Write the VHDL for the given circuit. Synthesize your circuit. (Run Synthesis).
✓ With a 100 MHz input clock, write the VHDL testbench.
 - To avoid long simulation times, use `ncols=4x4`, `ncols=1` and `COUNT_SCLKHP = SCLK_T/2= 2` for simulation purposes (resynthesize your circuit).
 - Generate the following input stream (4x4 16-bit words) to be captured at the rising edge of SCLK: 1110 1100 1110 1011 0100 0111 0001 0000 1010 1100 1110 1101 1110 1010 0101 0001 and then just 1's. The 16-bit values stored in memory should be: ECEB 4710 ACED EA51 FFFF ... FFFF. Verify that these values appear on the memory output on state S5. Place the `state` and `RAM_address` on the Simulator Wave Window. Run the simulation for 21 us.
- ✓ Perform Functional Simulation (Run Simulation → Run Behavioral Simulation). **Demonstrate this to your TA.**
- ✓ I/O Assignment: Create the XDC file.
Use `CLK100MHZ` for the input *clock*, `CPU_RESET` push button for *resetrn*, `LED0` for *ready_out*, `BTNC` for *start*, `M_CLK` for *SCLK*, `M_DATA` for *PDM_IN*, `M_LRSEL` for *LR*, `AUD_PWM` for *AUD_PWM*, `AUD_SD` for *AUD_SD*.
- ✓ Implement your design (Run Implementation).
- ✓ Do Timing Simulation (Run Simulation → Run Post-Implementation Timing Simulation). **Demonstrate this to your TA.**
- ✓ Generate and download the bitstream on the FPGA. Test the circuit: press *start* and record an audio sequence for 3.52 seconds. After that, the audio sequence is played back (use a headphone/speaker). **Demonstrate this to your TA.**
- Submit (as a .zip file) the generated files: VHDL code, and VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

TA signature: _____

Date: _____